AFW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	Docket No: SUNMP234
CHONG et al.	)	Group Art Unit: 2186
Application No: 10/623,083	)	Examiner: Bataille, Pierre Miche
Filed: July 17, 2003	)	Date: March 27, 2007
For: Time Slicing Device for Shared Resources and Method for Operating the Same	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on **March 27, 2007.**

Signed: _____
Kenneth D. Wright

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION -- 37 CFR 192)

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is in furtherance of the Notice of Appeal filed in this case on February 6, 2007 (mailed on January 29, 2007). This Appeal Brief is submitted within the two month time period for reply extending to April 6, 2007.

This application is on behalf of:

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

☐ $250.00 (Small Entity) ☒ $500.00 (Large Entity)

☐ Appeal Brief Fee has already been paid. Prosecution was re-opened by Examiner in response to the Appeal Brief, filed _____.

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Months	Large Entity	Small Entity
☐ one	$120.00	$60.00
☐ two	$450.00	$225.00
☐ three	$1,020.00	$510.00
☐ four	$1,590.00	$795.00

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for __ months has already been secured and the fee paid therefore of $ is deducted from the total fee due for the total months of extension now requested.

☒ Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Total Fees Due:

Appeal Brief Fee	$500.00
Extension Fee (if any)	$
Total Fee Due	**$500.00**

☒ Enclosed is Check No. 18057 in the amount of $500.00.

☐ The Commissioner is authorized to charge the total fees due of $___ to Deposit Account No. 50-0850, (Order No. _____).

☒ The Commissioner is authorized to charge any additional required fees or credit any overpayment to Deposit Account No. 50-0850, (Order No. SUNMP234).

One additional copy of this transmittal is enclosed for fee processing.

Respectfully submitted,
MARTINE PENILLA & GENCARELLA, LLP

Kenneth D. Wright
Reg. No. 53,795

710 Lakeway Drive, Suite 200
Sunnyvale, CA 94085
(408) 749-6900
Customer No. 32,291

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE CHONG ET AL.

Application for Patent

Filed July 17, 2003

Application No. 10/623,083

FOR:

Time Slicing Device for Shared Resources and Method for Operating the Same

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APPEAL BRIEF

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Signed: _____

Kenneth D. Wright

MARTINE PENILLA & GENCARELLA, LLP
Attorneys for Applicants

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I. REAL PARTY IN INTEREST

The real party in interest is Sun Microsystems, Inc., the assignee of the present application.

II. RELATED APPEALS AND INTERFERENCES

The Applicants are not aware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

A total of 22 claims were presented during prosecution of this application. The Applicants appeal rejected claims 1-22.

IV. STATUS OF THE AMENDMENTS

Original claims 1-22 remain pending. A Response without claim amendment was filed on June 1, 2006, in reply to the Office Action of March 1, 2006. A Request for Reconsideration without claim amendment was filed on October 23, 2006, in reply to the Final Office Action of August 21, 2006. Per the Advisory Action of November 30, 2006, the Examiner did not consider the Applicants' arguments in this Request for Reconsideration to be persuasive.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites one embodiment of the present invention directed to a device for addressing a shared resource (Figures 1-2, page 7, lines 4-5). The device includes at least one register in communication with the shared resource (Figures 1-2, page 7, lines 5-18). The at least one register is configured to hold an address to be provided to the shared resource upon receipt of a clock signal (Figures 1-2, page 9, lines 3-6). The device also includes a multiplexer for providing a next address to the at least one register

(Figures 1-2, page 7, lines 19-25). The multiplexer is disposed outside of a critical timing path for addressing the shared resource (Figures 1-2, page 10, lines 4-24).

Independent claim 8 recites one embodiment of the present invention directed to a shared memory (Figures 1-2, page 9, lines 14-16). The shared memory includes a data port for sending and receiving data (Figures 1-2, page 9, lines 1-3). The shared memory also includes an address port for receiving an address to be used to locate data within the shared memory (Figures 1-2, page 9, lines 3-6). The shared memory further includes at least one register in communication with the address port (Figures 1-2, page 9, lines 3-13). The at least one register is configured to provide the address to the address port upon receipt of a clock signal (Figures 1-2, page 9, lines 3-6). Additionally, the shared memory includes a multiplexer for providing a next address to the at least one register (Figures 1-2, page 7, lines 19-25). The multiplexer is disposed outside of a critical timing path for addressing the shared memory (Figures 1-2, page 10, lines 4-24).

Independent claim 15 recites one embodiment of the present invention directed to a method for addressing a shared resource (Figure 3, page 10, lines 11-13). The method includes an operation for loading at least one register with an address to be provided to the shared resource (Figure 3, page 10, lines 13-15). The method also includes an operation for providing the address to the shared resource from the at least one register upon receipt of a clock signal (Figure 3, page 11, lines 3-5).

It should be appreciated that the above discussion represents only a summary of the present invention. A more in-depth discussion of the present invention is provided in the Detailed Description section of the application.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 8, 15, and 21-22 were rejected under 35 U.S.C. 102(b) as being anticipated by Bennett (U.S. Patent No. 5,404,464). These rejections are traversed.

Claims 2-4, 9-11, and 16-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett in view of Lawrence (U.S. Patent No. 5,068,822), in view of Persoon et al. ("Persoon" hereafter) (U.S. Patent No. 4,627,021), and further in view of Farnsworth et al. ("Farnsworth" hereafter) (U.S. Patent No. 4,396,915). These rejections are traversed.

Claims 5-7 and 12-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett, in view of Ruetz (U.S. Patent No. 5,005,120). These rejections are traversed.

Claims 19-20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bennett, in view of Ruetz. These rejections are traversed.

VII. ARGUMENTS

A. Rejections of claims 1, 8, 15, and 21-22 under 35 U.S.C. 102(b) as being anticipated by Bennett

Independent Claim 1

Claim 1 was rejected under 35 U.S.C. 102 as being anticipated by Bennett. The following clear errors in the Examiner's rejection are noted.

1. **Bennett does not teach a multiplexer for providing a next address to at least one register in communication with a shared resource, wherein the multiplexer is disposed outside of a critical timing path for addressing the shared resource.**

The Examiner has asserted that the multiplexer (56) of Bennett teaches the multiplexer of claim 1. However, at a minimum, the multiplexer 56 of Bennett does not teach the feature of claim 1 requiring the multiplexer to be disposed outside of a critical timing path for addressing the shared resource. Figure 4 of Bennett and the associated discussion teach that Bennett's multiplexer 56 is connected between the address bus 70 and the early address signal line 84 that communicates with the bus controller 36. Bennett teaches that the early address signal to be provided to the bus controller 36 cannot be generated until the multiplexer 56 provides input to the Slot I.D. Mapping SRAM 60 so that the Last Slot I.D. Register 62 can be set. Therefore, it should be appreciated that the multiplexer 56 of Bennett is in fact disposed within the critical timing path for addressing the shared memory module 14.

The Examiner has referred to the teachings of Bennett at (6:40-44) as anticipating the feature of claim 1 requiring the multiplexer to be disposed outside of a critical timing path for addressing the shared resource. However, beyond simply quoting Bennett (6:40-

44) the Examiner provides no further explanation as to how Bennett (6:40-44) is being interpreted to teach the multiplexer disposed outside of a critical timing path for addressing the shared resource, as required by claim 1.

Simply stated, Bennett (6:40-44) does not teach or suggest that the multiplexer 56 is disposed outside of a critical timing path for addressing the memory module 14. Therefore, at a minimum, the Examiner's assertions regarding the teachings of Bennett do not satisfy the standard for lack of novelty (i.e., "anticipation") under 35 U.S.C. 102 as being that of strict identity. Moreover, the teachings of Bennett (6:40-44) actually indicate that the multiplexer 56 is in fact disposed within the critical timing path for addressing the memory module 14. In view of the foregoing, the Applicants submit that the multiplexer 56, as taught by Bennett, does not teach the multiplexer as required by claim 1. Additionally, the Applicants do not find another teaching in Bennett that would anticipate the multiplexer of claim 1.

Furthermore, as discussed below, Bennett does not teach at least one register in communication with a shared resource, wherein the at least one register is configured to hold an address to be provided to the shared resource upon receipt of a clock signal. Therefore, in addition to the above-discussed failing of Bennett to teach the multiplexer of claim 1, it should be appreciated that because Bennett does not teach the at least one register of claim 1, it is not reasonable to conclude that Bennett teaches a multiplexer for providing a next address to the at least one register.

It is well-established that the standard for lack of novelty (i.e., "anticipation") under 35 U.S.C. 102 is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *See, e.g., Hybritech Inc. v. Monoclonal Antibodies, Inc.,* 802 F.2d 1367, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1986). "A claim is anticipated only if each and every element as set forth in the claim is found, either

expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Additionally, "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In view of the foregoing, the Applicants submit that Bennett fails to teach each and every feature of independent claim 1, as required for anticipation under 35 U.S.C. 102. Therefore, the Applicants submit that independent claim 1 is not anticipated under 35 U.S.C. 102 by Bennett. Thus, the Applicants respectfully submit that the Examiner's rejection of claim 1 under 35 U.S.C. 102 is in error, and respectfully request that the Board of Patent Appeals and Interferences ("Board" hereafter) reverse the Examiner's rejection of claim 1.

2. Bennett does not teach at least one register in communication with a shared resource, wherein the at least one register is configured to hold an address to be provided to the shared resource upon receipt of a clock signal.

With regard to claim 1, the Examiner has asserted that Bennett teaches at least one register in communication with a shared resource, wherein the at least one register is configured to hold an address to be provided to the shared resource upon receipt of a clock signal. More specifically, the Examiner has asserted that the Last Slot ID Register (62) in the Bandwidth Maximizer Circuit (38) of Bennett teaches the at least one register of claim 1. However, the Applicants submit that the Last Slot ID Register (62) of Bennett does not teach the register configured to hold an address to be provided to a shared resource upon receipt of a clock signal, as required by claim 1.

Bennett (7:43-49) teaches that the Last Slot ID Register (62) is configured to hold, i.e., store, the "Slot ID" of the last address request that was made. Bennett (6:2-7) teaches that the "Slot ID" represents the slot number of a memory module (14), as opposed to an address to be provided to a shared resource. Bennett teaches that the "Slot ID" of the last address request is actually the slot number of the memory module (14) that contains the last address that was requested. It should be appreciated that the "Slot ID" as taught by Bennett is not equivalent to an address. This fact is further clarified in the following discussion provided by Bennett at (6:50-61):

> "In the present embodiment, the system memory is divided into blocks of 1 megabyte each. Thus, the slot numbers stored in each location of the slot I.D. mapping SRAM 60 are assigned on the basis of the 1-megabyte divisions of memory. For example, if the first megabyte of memory is mapped to a memory module 14 in slot 3 and the second megabyte of memory is mapped to a memory module 14 installed in slot 4, the computer operating system stores the identifier "3" (011 in binary) in the first location of the slot I.D. mapping SRAM 60, and the identifier "4" (100 in binary) in the second location of the slot I.D. mapping SRAM 60."

In view of the foregoing, the Applicants submit that the Last Slot ID Register (62), as taught by Bennett, does not teach the register configured to hold an address to be provided to a shared resource upon receipt of a clock signal, as required by claim 1. Rather, Bennett teaches that the Last Slot ID Register (62) is configured to store a memory module slot number. Additionally, the Applicants do not find another teaching in Bennett that would anticipate the register of claim 1.

In asserting that Bennett teaches the register configured to hold an address to be provided to a shared resource upon receipt of a clock signal, as required by claim 1, the

Examiner points to Bennett's teachings at column 8, lines 13-28. Specifically, the Examiner identifies Bennett as teaching the following: "The initiating CPU does not issue a strobe on the SADDS-signal line 44 until it enables the address bus 16." The Examiner asserts that this disclosure by Bennett teaches the register configured to hold an address to be provided to a shared resource upon receipt of a clock signal, as required by claim 1. The Applicants disagree.

The teachings of Bennett at column 8, lines 13-28, do not mention a register in communication with a shared resource, particularly wherein the register is configured to hold an address to be provided to the shared resource upon receipt of a clock signal. At a minimum, the Examiner's characterization of Bennett is an extrapolation of what is actually disclosed by Bennett. Therefore, the Examiner's assertions regarding the teachings of Bennett do not satisfy the standard for lack of novelty (i.e., "anticipation") under 35 U.S.C. 102 as being that of strict identity.

Additionally, the Examiner has explicitly stated that no consideration is given to the recited feature of claim 1 which requires that the at least one register be configured to hold an address to be provided to the shared resource upon receipt of a clock signal. The Examiner has stated that "the claims simply require a register." The Applicants disagree. Claim 1 requires that the at least one register be configured to hold an address to be provided to the shared resource upon receipt of a clock signal. With regard to the at least one register of claim 1, the "configured to" phrase serves to recite how the at least one register is configured within the device for addressing a shared resource. Therefore, the Applicants submit that it is not appropriate for the Examiner to simply ignore the claimed featured of "the at least one register configured to hold an address to be provided to the shared resource upon receipt of a clock signal."

Again, it is well-established that the standard for lack of novelty (i.e., "anticipation") under 35 U.S.C. 102 is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements. *See, e.g., Hybritech Inc. v. Monoclonal Antibodies, Inc.,* 802 F.2d 1367, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1986). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Additionally, "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In view of the foregoing, the Applicants submit that Bennett fails to teach each and every feature of independent claim 1, as required for anticipation under 35 U.S.C. 102. Therefore, the Applicants submit that independent claim 1 is not anticipated under 35 U.S.C. 102 by Bennett. Thus, the Applicants respectfully submit that the Examiner's rejection of claim 1 under 35 U.S.C. 102 is in error, and respectfully request that the Board reverse the Examiner's rejection of claim 1.

Independent Claim 8

The Examiner has referred to the teachings of Bennett at (6:40-44) as anticipating the feature of claim 8 requiring that the multiplexer be disposed outside of a critical timing path for addressing the shared memory. Therefore, the arguments presented above with respect to the multiplexer recited in claim 1 are equally applicable to the multiplexer recited in claim 8.

Also, with regard to claim 8, the Examiner has asserted that Bennett teaches at least one register configured to provide an address to an address port of a shared memory

upon receipt of a clock signal. More specifically, the Examiner has asserted that claim 5 of Bennett (17:5-19) teaches the register of claim 8. The static random access memory recited in claim 5 of Bennett corresponds to the Slot I.D. Mapping SRAM 60 in the Bandwidth Maximizer Circuit (38) of Bennett. Also, the storage register recited in claim 5 of Bennett corresponds to the Last Slot I.D. Register 62 in the Bandwidth Maximizer Circuit (38) of Bennett. Therefore, the arguments presented above with respect to the at least one register in communication with a shared resource as recited in claim 1 are equally applicable to the at least one register recited in claim 8.

In view of the foregoing, the Applicants submit that Bennett fails to teach each and every feature of independent claim 8, as required for anticipation under 35 U.S.C. 102. Therefore, the Applicants submit that independent claim 8 is not anticipated under 35 U.S.C. 102 by Bennett. Thus, the Applicants respectfully submit that the Examiner's rejection of claim 8 under 35 U.S.C. 102 is in error, and respectfully request that the Board reverse the Examiner's rejection of claim 8.

Independent Claim 15

With regard to claim 15, the Examiner has asserted that Bennett (8:13-28) teaches loading at least one register with an address to be provided to the shared resource, and providing the address to the shared resource from the at least one register upon receipt of a clock signal. Once again, the Examiner has referred to the Last Slot I.D. Register 62 in the Bandwidth Maximizer Circuit (38) of Bennett as teaching the register loaded with an address to be provided to a shared resource upon receipt of a clock signal, as required by claim 15. As previously discussed with respect to claim 1, the Last Slot ID Register (62) of Bennett is configured to store a "Slot ID" of the last address request that was made, wherein the "Slot ID" represents the slot number of a memory module (14). It should be

appreciated that the "Slot ID" is not an address to be provided to a shared resource, i.e., to a shared memory. Therefore, the arguments presented above with respect to the at least one register in communication with a shared resource as recited in claim 1 are equally applicable to claim 15.

In view of the foregoing, the Applicants submit that Bennett fails to teach each and every feature of independent claim 15, as required for anticipation under 35 U.S.C. 102. Therefore, the Applicants submit that independent claim 15 is not anticipated under 35 U.S.C. 102 by Bennett. Thus, the Applicants respectfully submit that the Examiner's rejection of claim 15 under 35 U.S.C. 102 is in error, and respectfully request that the Board reverse the Examiner's rejection of claim 15.

Dependent Claims 21 and 22

Because a dependent claim incorporates each and every feature of its independent claim, the Applicants submit that each of dependent claims 21 and 22 is patentable for at least the same reasons provided for claim 15. Therefore, the Applicants respectfully submit that the Examiner's rejections of dependent claims 21 and 22 under 35 U.S.C. 102 are in error, and respectfully request that the Board reverse the Examiner's rejections of claims 21 and 22.

B. Rejections of claims 2-4, 9-11, and 16-18 under 35 U.S.C. 103(a) as being unpatentable over Bennett in view of Lawrence, in view of Persoon, and further in view of Farnsworth

Because a dependent claim incorporates each and every feature of its independent claim, the Applicants submit that each of dependent claims 2-4, 9-11, and 16-18 is patentable with respect to the cited art of record for at least the same reasons provided for its respective independent claim. Therefore, the Applicants respectfully submit that the

Examiner's rejections of dependent claims 2-4, 9-11, and 16-18 under 35 U.S.C. 103 are in error, and respectfully request that the Board reverse the Examiner's rejections of claims 2-4, 9-11, and 16-18.

C. Rejections of claims 5-7 and 12-14 under 35 U.S.C. 103(a) as being unpatentable over Bennett in view of Ruetz

Because a dependent claim incorporates each and every feature of its independent claim, the Applicants submit that each of dependent claims 5-7 and 12-14 is patentable with respect to the cited art of record for at least the same reasons provided for its respective independent claim. Therefore, the Applicants respectfully submit that the Examiner's rejections of dependent claims 5-7 and 12-14 under 35 U.S.C. 103 are in error, and respectfully request that the Board reverse the Examiner's rejections of claims 5-7 and 12-14.

D. Rejections of claims 19 and 20 under 35 U.S.C. 103(a) as being unpatentable over Bennett in view of Ruetz

Because a dependent claim incorporates each and every feature of its independent claim, the Applicants submit that each of dependent claims 19 and 20 is patentable for at least the same reasons provided for claim 15. Therefore, the Applicants respectfully submit that the Examiner's rejections of dependent claims 19 and 20 under 35 U.S.C. 102 are in error, and respectfully request that the Board reverse the Examiner's rejections of claims 19 and 20.

Conclusion

In view of the foregoing, the Applicants submit that each of claims 1-22 is patentable. Therefore, the Applicants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's rejections of the claims on appeal.

Respectfully Submitted,
MARTINE PENILLA & GENCARELLA, LLP

Kenneth D. Wright
Reg. No. 53,795

MARTINE PENILLA & GENCARELLA, LLP
710 Lakeway Drive, Suite 200
Sunnyvale, California 94085
408.749.6900

VIII. CLAIMS APPENDIX

1. A device for addressing a shared resource, comprising:

at least one register in communication with the shared resource, the at least one register configured to hold an address to be provided to the shared resource upon receipt of a clock signal; and

a multiplexer for providing a next address to the at least one register, the multiplexer being disposed outside of a critical timing path for addressing the shared resource.

2. A device for addressing a shared resource as recited in claim 1, wherein the multiplexer is configured to receive a recirculate input, an increment input, a new address input, and a control signal, the control signal being used to determine which of the recirculate input, the increment input, and the new address input is to be provided as the next address to the at least one register.

3. A device for addressing a shared resource as recited in claim 2, wherein the new address input is provided in a time multiplexed manner to cause the at least one register to provide the address to the shared resource upon receipt of a specific clock signal.

4. A device for addressing a shared resource as recited in claim 2, wherein the new address input is provided by one of a multiple input multiplexer, a memory manager module, and a buffer allocator module, each of the multiple input multiplexer, the memory manager module, and the buffer allocator module existing outside of the critical timing path for addressing the shared resource.

5. A device for addressing a shared resource as recited in claim 1, wherein the at least one register includes a register chain, the register chain being defined by a number of registers connected in a serial manner, the number of registers including a first register and a last register, the first register being provided with the next address from the multiplexer.

6. A device for addressing a shared resource as recited in claim 5, wherein each of the number of registers has an input and an output, the output of each register that is not the last register in the register chain being connected to the input of a sequential register in the register chain to define the serial manner of connection, the output of the last register in the register chain being connected to an input of the multiplexer.

7. A device for addressing a shared resource as recited in claim 5, wherein each of a number of portions of the shared resource is provided with one of a number of addresses from the output of the number of registers in the register chain upon receipt of the clock signal.

8. A shared memory, comprising:

a data port for sending and receiving data;

an address port for receiving an address to be used to locate data within the shared memory;

at least one register in communication with the address port, the at least one register configured to provide the address to the address port upon receipt of a clock signal; and

a multiplexer for providing a next address to the at least one register, the multiplexer being disposed outside of a critical timing path for addressing the shared memory.

9. A shared memory as recited in claim 8, wherein the multiplexer is configured to receive a recirculate input, an increment input, a new address input, and a control signal, the control signal being used to determine which of the recirculate input, the increment input, and the new address input is to be provided as the next address to the at least one register.

10. A shared memory as recited in claim 9, wherein the new address input is provided in a time multiplexed manner to cause the at least one register to provide the address to the address port upon receipt of a specific clock signal.

11. A shared memory as recited in claim 9, wherein the new address input is provided by one of a multiple input multiplexer, a memory manager module, and a buffer allocator module, each of the multiple input multiplexer, the memory manager module, and the buffer allocator module existing outside of the critical timing path for addressing the shared memory.

12. A shared memory as recited in claim 8, wherein the at least one register includes a register chain, the register chain being defined by a number of registers connected in a serial manner, the number of registers including a first register and a last register, the first register being provided with the next address from the multiplexer.

13. A shared memory as recited in claim 12, wherein each of the number of registers has an input and an output, the output of each register that is not the last register in the register chain being connected to the input of a sequential register in the register chain to define the serial manner of connection, the output of the last register in the register chain being connected to an input of the multiplexer.

14. A shared memory as recited in claim 12, wherein each of a number of portions of the shared memory is provided with one of a number of addresses from the output of the number of registers in the register chain upon receipt of the clock signal.

15. A method for addressing a shared resource, comprising:

loading at least one register with an address to be provided to the shared resource; and

providing the address to the shared resource from the at least one register upon receipt of a clock signal.

16. A method for addressing a shared resource as recited in claim 15, further comprising:

operating a multiplexer to load the at least one register with one of a recirculated address, an incremented address, and a new address.

17. A method for addressing a shared resource as recited in claim 16, further comprising:

operating one of a multiple input multiplexer, a memory manager module, and a buffer allocator module to provide the new address to the multiplexer, wherein the

multiple input multiplexer, the memory manager module, and the buffer allocator module are operated outside of a critical timing path for providing the address to the shared resource.

18. A method for addressing a shared resource as recited in claim 15, wherein a critical timing path for providing the address to the shared resource is defined by propagation of the clock signal to the at least one register and propagation of the address to the shared resource.

19. A method for addressing a shared resource as recited in claim 15, further comprising:

providing a register chain defined by the at least one register and a number of additional registers;

loading the number of additional registers with a number of additional addresses to be provided to the shared resource; and

providing each of the number of additional addresses to different portions of the shared resource from the number of additional registers upon receipt of the clock signal used to provide the address to the shared resource from the at least one register.

20. A method for addressing a shared resource as recited in claim 19, further comprising:

shifting the address and the number of additional addresses through the register chain to allow each of the address and the number of additional addresses to be provided to appropriate portions of the shared resource at a specific clock cycle.

21. A method for addressing a shared resource as recited in claim 15, wherein the shared resource is a shared memory.

22. A method for addressing a shared resource as recited in claim 15, wherein the address is provided directly to the shared resource from the at least one register upon receipt of the clock signal.

IX. EVIDENCE APPENDIX

There is currently no evidence entered and relied upon in this Appeal.

X. RELATED PROCEEDINGS APPENDIX

There are currently no decisions rendered by a court or the Board in any proceeding identified in the Related Appeals and Interferences section.